

40W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

- VIN Input Voltage Range: 4.2V-30V
 - PVIN Input Voltage Range: 1V~26V
 - Up to 40W Power Transfer
 - Integrated Full-Bridge Power Stage with 13-m R_{ds(on)} of Power MOSFETs
 - Integrated High Efficiency 5V-1A Step-down DC/DC Converter
 - Build-in 3.3V-200mA LDO
 - Integrated Lossless Input Current Sensor with $\pm 2\%$ accuracy for FOD and current Demodulation
 - Integrated voltage and current demodulation
 - Integrated Q factor detection
 - 3.3V and 5V PWM Signal Logic Compatible
 - Input Under-Voltage Lockout
 - Over Current Protection
 - Over Temperature Protection
 - Available in QFN-22L 4mm*4mm Package
- WPC EPP Chargers of 10W to 40W Systems for Mobiles and tablets
 - General Wireless Power Transmitters for Consumer, Industrial and Medical Equipment
 - Proprietary Wireless Chargers and Transmitters

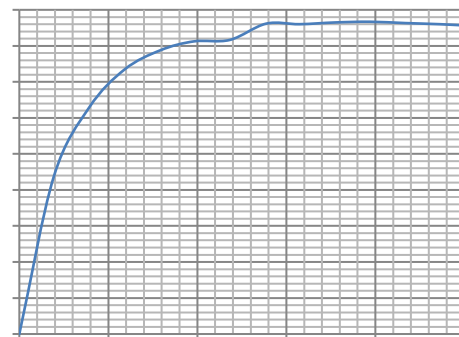
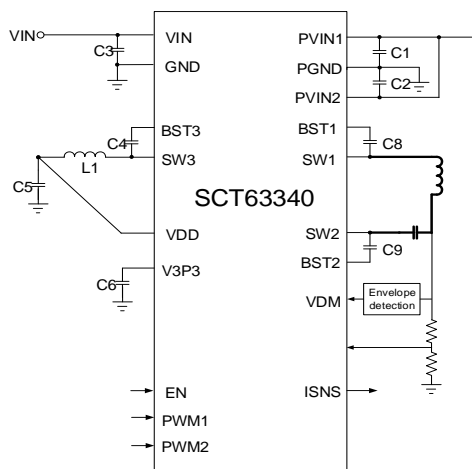
The SCT63340 is a highly integrated Power Management IC allows achieving high performance, high efficiency and cost effectiveness of wireless power transmitter system compliant with WPC specification to support up to 40W power transfer, working with a wireless application specific controller ASIC or a general MCU based transmitter controller.

This device integrates a 4-MOSFETs full bridge gate drivers, a 5V step-down DC/DC converter, a 3.3V LDO, communication demodulator, Q-factor detection and input current sensor for both system efficiency and easy-to-use.

The proprietary gate driving scheme optimizes the performance of EMI reduction to save the system cost and design. The proprietary lossless current sensing circuitry with $\pm 2\%$ accuracy monitors input current of full bridge to support Foreign Object Detection FOD and current demodulation. The build-in 5V step-down DC/DC converter and 3.3V low dropout regulator LDO can provide power supplies to transmitter controller and external circuitries.

The SCT63340 features input under-voltage lock-out UVLO protection, over current protection, short circuit protection, and over temperature protection for robust design.

The SCT63340 is available in a compact QFN 4mm*4mm package.



SW3	6	Switching output of the Buck converter. Connect SW3 to an external power inductor.
BST3	7	Power supply bias for the high-side power MOSFET gate driver of Buck converter. Connect a 0.1uF capacitor from BST3 pin to SW3 pin.
VDD	8	Output voltage of the Buck converter. Connect 22uF capacitor from this pin to GND

SCT63340

PARAMETER	THERMAL METRIC	FCTQFN4X4-22L	UNIT
R _{JA}	Junction to ambient thermal resistance ⁽¹⁾	40	°C/W
R _{JC}	Junction to case thermal resistance ⁽¹⁾	24	

(1) SCT provides R_{JA} and R_{JC} numbers only as reference to estimate junction temperatures of the devices. R_{JA} and R_{JC} are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63340 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63340. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R_{JA} and R_{JC}.

$V_{IN}=V_{PVIN1}=V_{PV}$

PWM1

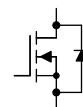


Figure 8. Functional Block Diagram

Overview

The SCT63340 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V buck converter as power supply for external transmitter controller and internal 5V power supply to increase system efficiency, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with $\pm 2\%$ accuracy, 3.3V output LDO for powering MCU.

The SCT63340 has four power input pins. VIN is connected to the power FETs of buck converter. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for transferring power. VDD is the output feedback pin of the 5V output buck converter meanwhile as the power supply for internal two LDOs and full bridge MOSFET's gate driver.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 30V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.18V typically. The maximum operating voltage for PVIN is up to 26V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gated drivers of full bridge MOSFETs. Full bridge power stage enables working when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63340 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The buck converter and full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off speed, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63340 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for buck converter and 4-MOSFETs full bridge, current limit and current fold back at hard short for the LDO and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 3.56V and the EN pin voltage exceeds the threshold of 1.19V, the buck converter and two LDOs enable. The device disables when the VIN pin voltage falls below 3.2V or when the t_{F1QEMC} /Sp

SCT63340

5V Output Buck Converter

The SCT63340 fully integrates synchronous buck converter with up to 30V input voltage and 5V fixed output voltage, which offers up to 1A output current capability. The device employs 450KHz fixed frequency peak current mode control with the internal loop compensation network and built-in 1.4ms soft-start which makes this buck converter easily to be used by minimizing the off-chip component count. Pulse Skipping Modulation(PSM) is adopted to increase the light load efficiency.

The buck converter's output, a fixed 5V voltage, supports the power requirement on system such as transmitter controller or mechanical fan meanwhile it is also the power supply of the SCT63340's 3.3V LDO and gate drivers of 4-MOSFETs full bridge. Connect 22uF capacitor from VDD to GND and add a 0.1uF local bypass ceramic capacitor placed close to the IC.

The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further eras

SCT63340

The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure10. This simple implementation achieves the envelope detector function, low-pass filter as well as the DC filter function. The envelope detector applies the analog signal to VDM pin and the chip do the demodulation and output a digital signal to VDMO pin which MCU can capture the voltage demodulation results and then implement the packet decode.

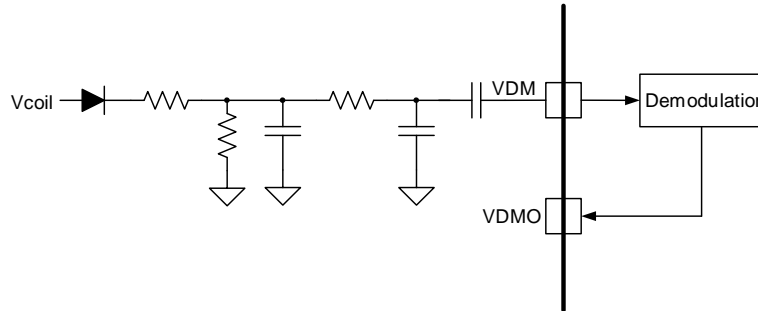


Figure 10. Envelope Detector

The current-mode detector takes the modulation information from the average input current which the chip can read from ISNS pin. The MCU can detect the demodulation results and then implement the packet decode.

Layout Guideline

Proper PCB layout is a critical for SCT63340's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Buck converter output capacitor's ground should connect to GND directly to minimize the power loop.
5. VDD pin can connect to the DC/DC's output capacitor from bottom layer, connect to the point behind the capacitor while not connect to inductor.
6. Bypass capacitor for VDD place next to VDD pin.
7. Bypass capacitor for V3P3 place next to V3P3 pin.

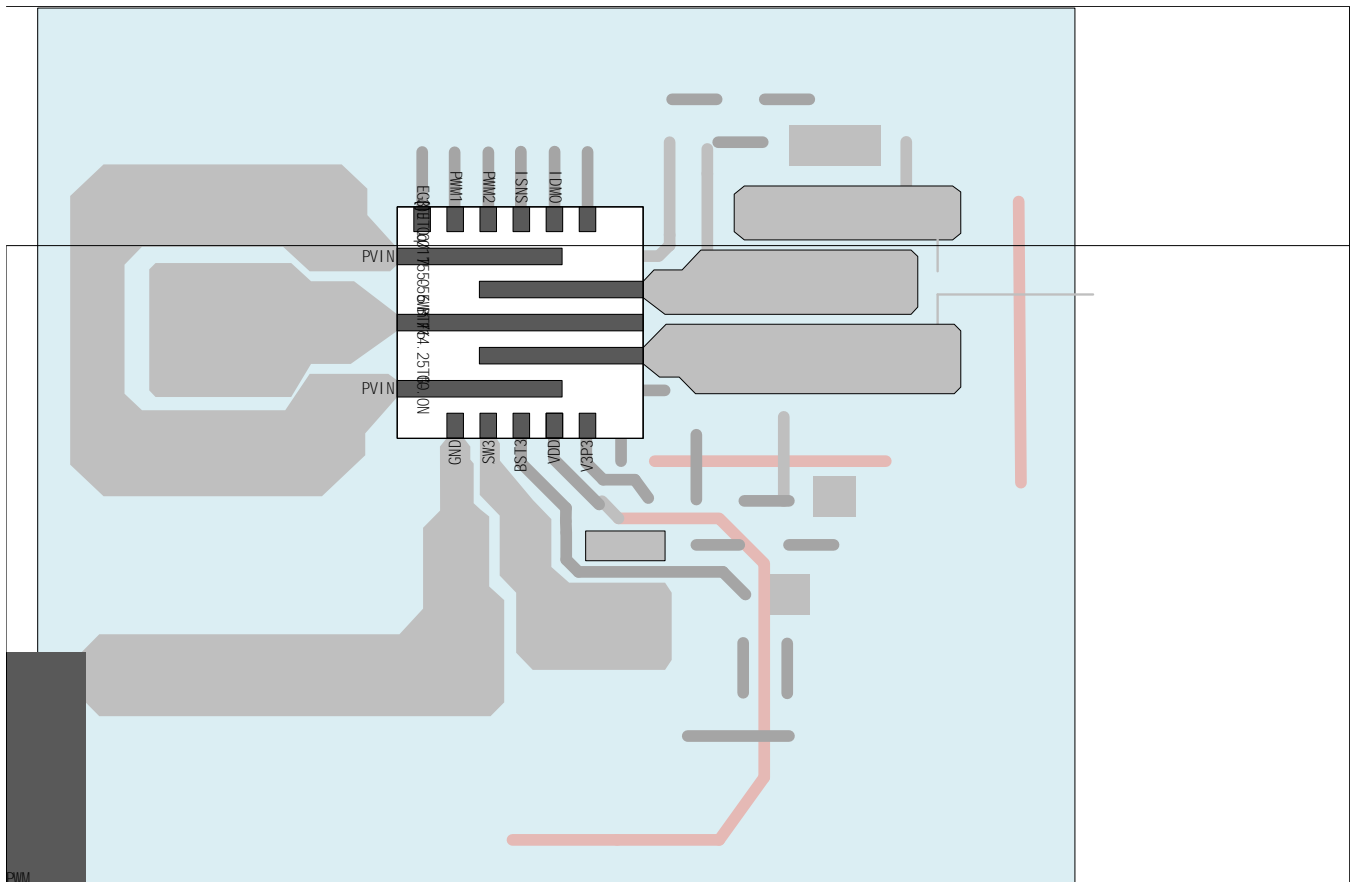
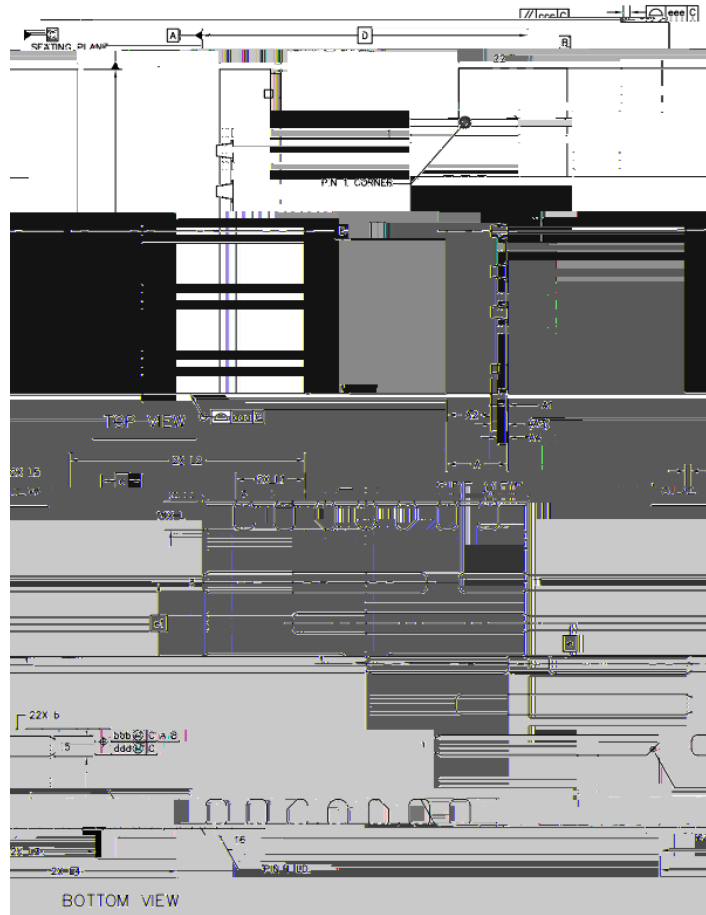


Figure 18. PCB Layout Example



FCTQFN-22L (4x4) Package Outline Dimensions

STANDARD	MIN	EXAMPLE	MAX	UNIT
STANDARD OFF	0	0.25	0.25	mm
STANDARD P/P	0	0.25	0.25	mm
STANDARD P/P	0	0.25	0.25	mm
SIDE-WETTABLE-DEPTH	0.075			mm
LEAD				mm
BEZEL	4-BSC			
PITCH	0.5			mm
	0.35	0.4		mm
LEAD LENGTH	L1	2.85	2.9	2.95
	L3	1.7	1.75	1.8
	L4	2.7	2.75	2.8
FACE EDGE TOLERANCE	ccc	0.1		mm
FLATNESS	ccc	0.1		mm
LEAD OFFSET				mm

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

